Pattern Verification and Generator User's Guide

This document provides instruction on enabling the pattern generator and pattern verification functions of the SNx5DP159/SNx5DP149 and TMDS181/TMDS171 devices to aid in the HDMI and DP++ system debug and verification.

1 Overview

1.1 Pattern Generator

The SNxDP159/DP149 and TMDS181/171 devices have a test pattern generator on each TX lane. These pattern generators support several standard pseudo-random bit stream (PRBS) sequences, as well as clock pattern and user-defined custom patterns. Custom patterns are outside the scope of this document. The type of pattern to be transmitted is specified by the pg_sel input control bus, as shown in Table 1. When PRBS is selected as the transmit test pattern, the specific PRBS pattern is selected by the pg_len input control bus. The generated PRBS patterns conform to the generally accepted test equipment requirements. The SNxDP159/DP149 and TMDS181/171 devices require an external clock to be provided on the receiver (IN_CLKn/IN_CLKp) to generate test patterns.

Table 1. TX Pattern Generator Control / Status Register Fields

Address (Page 1)	Bits	Description
18h	7:4	PV_SYNC[3:0]. Pattern timing pulse. This field is updated for 8UI once every cycle of the PRBS generator. 1 bit per lane.
	3:0	PG_LD[3:0]. Load pattern-generator controls into TX lane. When asserted high, the PG_TO, PG_SEL, PG_LEN, PG_CP20, and PG_CP values are enabled into the corresponding TX lane. These values are then latched and held when PG_LD[n] is subsequently deasserted low. 1 bit per lane.
19h	7:4	Reserved
	3:0	PG_ERR_INJ[3:0]. Inject error into pattern. Upon the rising edge of PG_ERR_INJ[n], an error is inserted into the transmitted pattern of the corresponding lane.
1Ah	7	PG_CP20. Custom pattern length 20/16 bits. 0 – 16 bits 1 – 20 bits
	6	Reserved
	5	PG_TO. Pattern generator timing-only mode - set to 0.
	4:2	PG_LEN[2:0]. PRBS pattern length 000 – PRBS7 001 – PRBS11 010 – PRBS23 011 – PRBS31 100 – PRBS15 101 – PRBS15 110 – PRBS20 111 – PRBS20
	1:0	PG_SEL[1:0]. Pattern select. 00 – Disabled 01 – PRBS based on PG_LEN[2:0] 10 – Clock pattern 11 – Not Supported

1.2 Register Setting Example:

```
(0xFF, 0x00); // Select Page 0
(0x0B, 0xXX); // Set TMDS_CLOCK_RATIO_STATUS to 1/10 for HDMI 1.4B and 1/40 for HDMI 2.0 data
rates
(0x0A, 0xB7); // Set to retimer mode and apply changes
(0xFF, 0x01); // Select Page 1
(0x1A, 0x01); // Select PRBS7 as the pattern
(0x18, 0x07); // Load pattern on lanes 0 thru 2, leave the clock lane
(0x18, 0x00); // Load is latched
```

1.3 Pattern Verification

The SNxDP159/DP149 and TMDS181/171 devices have a pattern verification functions on each RX lane. The pattern verification functions supports several standard pseudo-random bit stream (PRBS) sequences, as well as clock pattern and user-defined custom patterns. Custom patterns are outside the scope of this document. The pattern verification functions are controlled by the pv_sel[2:0], pv_len[2:0], pv_cp20, and pv_thr[2:0] control inputs. Although these controls are common to all lanes, they are only loaded into any particular RX lane i when the corresponding pv_ld[i] bit is asserted high. These values are then latched and held in the RX lane when pv_ld[i] is subsequently deasserted low.

When the pattern verification function is first enabled it will attempt to train to the incoming data pattern. During this training process, incoming data is collected into an internal pattern comparator/generator so as to initialize its pattern state and the pv_tip output is asserted high. When enough data has been collected to initialize the pattern comparator, the pv_tip output is deasserted, the internal pattern comparator runs autonomously, and pattern verification begins.

When a mismatch between the incoming data and the expected pattern occurs, the pv_fail output is asserted. If the number of consecutive failures exceeds the threshold specified by the pv_thr input control bus, then the training process is restarted.

NOTE: If pv_thr is 0, then the first mismatch detected causes training to be restarted.

Pattern errors accumulate in bert_cnt. The BERT counters is cleared by setting bert_clr.

When PRBS is selected as the received test pattern, the specific PRBS pattern is selected by the pv_len input control bus, as shown in Table 2. The received PRBS patterns must conform to the generally accepted test equipment requirements.

Table 2. RX Pattern Verification Control / Status Register Fields

Address (Page 0)	Bits	Description
0Eh	7:4	PV_SYNC[3:0]. Pattern timing pulse. This field is updated for 8UI once every cycle of the PRBS generator. 1 bit per lane.
	3:0	PV_LD[3:0]. Load pattern-verifier controls into RX lanes. When asserted high, the PV_TO, PV_SEL, PV_LEN, PV_CP20, and PV_CP values are enabled into the corresponding RX lane. These values are then latched and held when PV_LD[n] is subsequently deasserted low. 1 bit per lane.
0Fh	7:4	PV_FAIL[3:0]. Pattern verification mismatch detected. 1 bit per lane
	3:0	PV_TIP[3:0]. Pattern search/training in progress. 1 bit per lane.

Table 2. RX Pattern Verification Control / Status Register Fields (continued)

Address (Page 0)	Bits	Description
10h	7	PV_CP20. Customer pattern length 20/16 bits. 0 – 16 bits (default) 1 – 20 bits
	6	Reserved
	5:3	PV_LEN[2:0]. PRBS pattern length 000 – PRBS7 (default) 001 – PRBS11 010 – PRBS23 011 – PRBS31 100 – PRBS15 101 – PRBS15 110 – PRBS20 111 – PRBS20
	2:0	PV_SEL[24:0]. Pattern select control 000 – Disabled (default) 001 – PRBS 010 – Clock 011 – Custom 1xx – Not Supported
14h	7:3	Reserved
	2:0	PV_THR[2:0] Pattern-verification retain threshold.
15h	7	DESKEW_CMPLT
	6	DESKEW_ERROR
	5	Reserved
	4	BERT_CLR. Clear BERT counter (on rising edge).
	3:0	Reserved
18h	7:0	BERT_CNT[7:0] BERT error count. Reflects Lane 0 (IN_D2p/IN_D2n) errors.
19h	7:4	Reserved
	3:0	BERT_CNT[11:8] BERT error count. Reflects Lane 0 (IN_D2p/IN_D2n) errors
1Ah	7:0	BERT_CNT[19:12] BERT error count. Reflects Lane 1 (IN_D1p/IN_D1n) errors
1Bh	7:4	Reserved
	3:0	BERT_CNT[23:20] BERT error count. Reflects Lane 1 (IN_D1p/IN_D1n) errors
1Ch	7:0	BERT_CNT[31:24] BERT error count. Reflects Lane 2 (IN_D0p/IN_D0n) errors
1Dh	7:4	Reserved
	3:0	BERT_CNT[35:32] BERT error count. Reflects Lane 2 (IN_D0p/IN_D0n) errors
1Eh	7:0	BERT_CNT[43:36] BERT error count. Reflects Lane 3 (IN_CLKp/IN_CLKn) errors
1Fh	7:4	Reserved
	3:0	BERT_CNT[47:44] BERT error count. Reflects Lane 3 (IN_CLKp/IN_CLKn) errors

1.3.1 Register Setting Example:

```
(0xFF, 0x00); // Select Page 0
(0x0B, 0xXX); // Set TMDS_CLOCK_RATIO_STATUS to 1/10 for HDMI 1.4B and 1/40 for HDMI 2.0 data
rates
(0x0A, 0xB7); // Set to retimer mode and apply changes
(0x10, 0x01); // Select PRBS7 as the pattern
(0x0E, 0x07); // Load pattern verification on lanes 0 thru 2 when SWAP disabled, leave the clock
lane
//(0x0E, 0x0E); // Load pattern verification on lanes 1 thru 3 when SWAP enabled, leave the clock
lane
(0x0E, 0x00); // Load is latched
```

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265