LMR54620 PSPICE Transient Model Features and Limitations

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* Model Usage Notes:
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* A. Features modelled
*   1. Programmable VOUT
*   2. Soft Start
*   3. PWRGD functionlality
*   4. BOOT function
*   5. Programmable Frequency(RT)
*   6. Input UnderVoltage LockOut(UVLO)
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* B. Features have not been modelled
*   1. Operating Quiescent Current
*   2. The SS_TR to VSENSE matching
*   3. Minimum VIN for valid PWRGD output
*   4. Minimum SS_TR voltage for PWRGD
*   5. Internal PLL for the RT_CLK pin
*   6. Switchover from RT mode to CLK mode
*   7. Temperature dependent characteristics
*   8. Ground pins have been tied to 0V internally. Therefore, this model cannot be used for inverting topologies.
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* C. Application Notes
*   1. The parameter SS has been used to reach the steady state faster.
*      Keep SS = 0 to observe startup behaviour.
*      Keep SS = 1 and appropriate IC on Inductor and capacitor to observe for faster Steady state.
*   2. The internal PLL for the RT_CLK pin has not been modeled and hence the switchover from RT mode to CLK
*      mode has not been modeled. However the model can operate in RT mode and CLK mode depending on the
*      resistor or clock signal connected to the RT_CLK pin.
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