TEXAS INSTRUMENTS

Choosing an ADC and Op Amp for Minimum Offset

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Contents

List of Figures

List of Tables

Choosing an ADC and Op Amp for Minimum Offset

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ABSTRACT

Designing a mixed-signal circuit containing analog and digital components can be a challenge to the development engineer. Requirements such as a low single-polarity supply voltage and a high degree of precision may conflict, and make the choice of components and the best circuit design difficult. This report discusses problems that arise in using operational amplifiers (op amps) for signal conditioning, and in interfacing a 10-bit A/D converter to a digital signal processor.

Background

Measurement and control applications increasingly use digital systems. However, all the variables that sensors measure (such as temperature, pressure or light intensity) are analog; therefore, an element is needed to link the analog environment to the digital system. This usually means that signals from sensors must be modified for conversion into a digital data format.

An operational amplifier (op amp) generally conditions the signal from a sensor. In the past, op amps used a bipolar supply voltage of ±15 V. The output voltage of such an op amp cannot swing between the maximum voltage levels of the supply; the maximum output voltage limits lie about 2 V above the negative supply voltage, and the same amount below the positive supply voltage. In the same way, the common-mode voltage applied to the input cannot reach the negative or positive supply voltages. In systems using bipolar ±15-V supplies however, this was not a particular restriction, because the remaining dynamic range still provided a wide dynamic range for the signal.

Unipolar Supplies and Op Amps

In most applications nowadays however, a unipolar supply voltage of 5 V, or—particularly with portable systems—a single supply of only 3 V is used.

In applications operating from a unipolar supply voltage, it is particularly important that it be possible to drive the op amp input down to 0 V, the ground (GND) voltage level. This makes it possible to amplify the very low-level signals from sensors.

CMOS op amps are ideally suited for this purpose. With the use of P-channel field-effect transistors in their input stages, the permissible common-mode voltage at the input can be taken down to the negative supply voltage, or to ground (GND) with a unipolar supply voltage. Figure 1 shows the input stage of a CMOS op amp from Texas Instruments.

The differential amplifier consists of P-channel field-effect transistors. Linear driving of the op amp is then only possible when $V_{GS} < V_T$ applies for the input voltage. As the input characteristics show, V_T is the threshold voltage of the field-effect transistor.

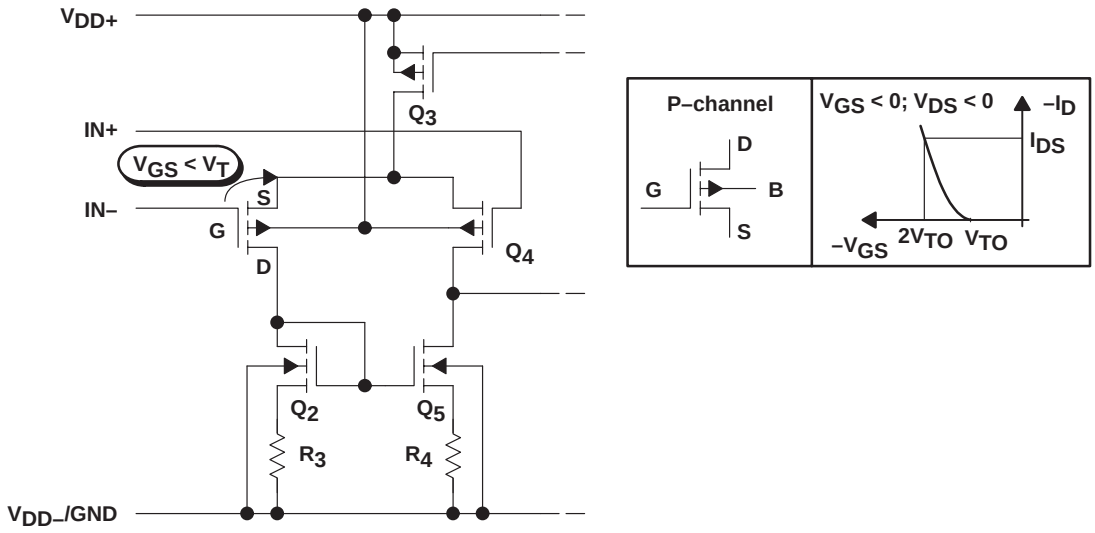

Figure 1. Input Stage of a CMOS Op Amp

With these conditions, it is permissible to drive the op amp down to V_{DD-} or GND. Driving in the positive direction is limited however, and the limit usually lies about 0.8 V to 1.5 V below the positive supply voltage.

This input stage has the advantage of a very high input resistance, making extremely low input currents attainable.

The magnitude of the positive supply voltage—the permissible driving dynamic range—and the sum of the total errors of the op amp limit the usable dynamic signal range of an op amp with a single supply voltage. Reducing the supply voltage from ±15 V to 5 V or 3 V reduces the maximum dynamic range, and thus the performance of the circuit. Figure 2 shows how the dynamic range of a typical linear component deteriorates when the supply voltage is reduced from ±15 V to 5 V, and then to 3 V.

It is important that as much as possible of the reduced supply voltage remains available for the usable dynamic range. Using components that can be driven and controlled up to the limits of the supply voltage can achieve this goal. This ability at the output of the op amp is called rail-to-rail compatibility.

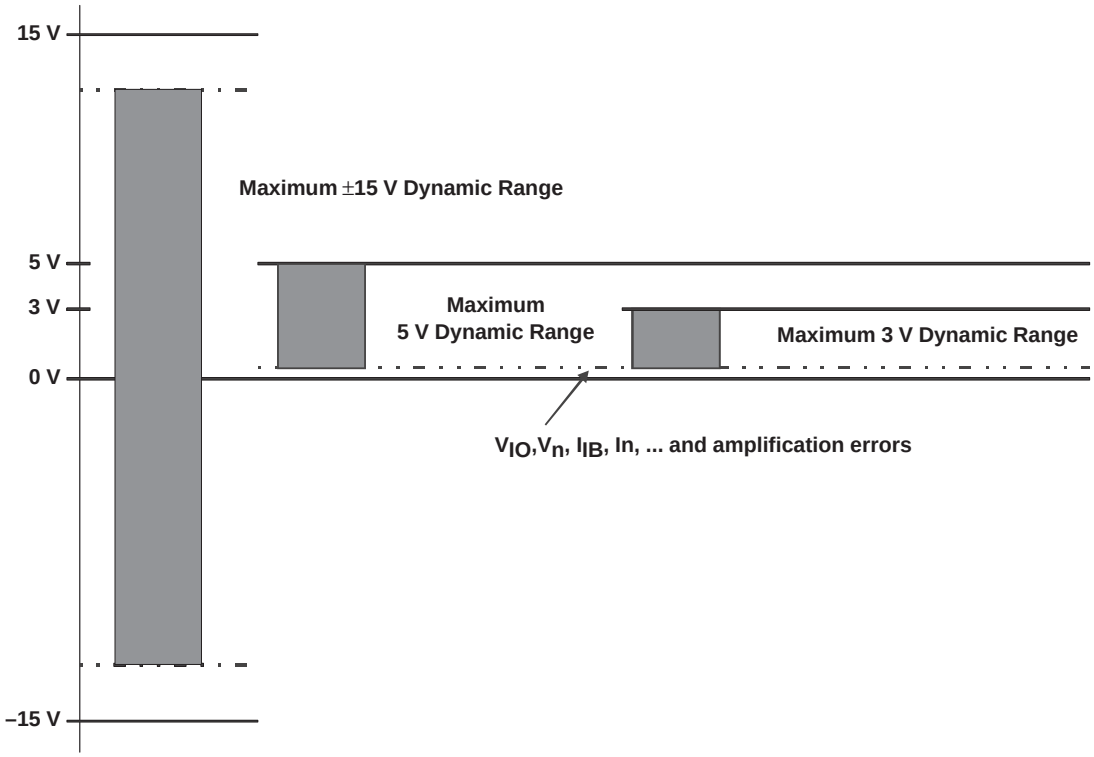

Figure 2. Dynamic Range

Texas Instruments provides a number of rail-to-rail op amps in Advanced-LinCMOS technology, for 5-V and 3-V systems.

Compared to bipolar technology, CMOS op amps have very low supply current. The resulting low power consumption makes them specially suited for battery operated systems.

CMOS Op Amps and Input Offset Voltage

CMOS technology has one disadvantage compared to bipolar components: the relatively high input offset voltage. CMOS op amps have a typical input offset voltage of a few millivolts. The op amp multiplies this input offset voltage, and it becomes an important parameter in determining the precision that can be achieved with the signal conditioning of direct current signals.

Table 1 shows the minimum resolvable potential difference (magnitude of the LSB) of A/D converters. If, for example, 12-bit precision is required in a 3-V system, then a change of the LSB corresponds to a voltage change of 0.73 mV. An op amp having an input offset voltage of 1 mV and an amplification factor of 1 already exceeds the acceptable error resulting from the resolution of the LSB.

Table 1. Resolution of an A/D Converter

BITS	STEPS	RESOLUTION AT V_{CC} = 5 V	RESOLUTION AT V_{CC} = 3 V	RESOLUTION IN %
10	1024	4.88 mV	2.93 mV	0.098
12	4096	1.22 mV	0.73 mV	0.024

Texas Instruments makes CMOS precision op amps that adddress this problem using chopper stabilisation (TLC2652 and TLC2654). Chopper op amps are used primarily to amplify direct current signals, and they have extremely low input offset voltages. An internally-clocked circuit interrogates and compensates the input offset voltage. This technique can achieve input offset voltages of only 1 μV. Even in 5-V systems with 12-bit resolution, it is possible to choose higher amplifications without the error from the input offset voltage becoming larger than that resulting from the resolution of the LSB. Disadvantages, however, are the need for external storage capacitors and a limited usable bandwidth.

Texas Instruments now offers a new technique (Self-Cal™) that limits the input offset voltage to 50 μV maximum without external circuitry. This technique allows the op amp to compensate the input offset voltage internally. The TLC4502 is the first CMOS op amp with this self-calibration feature. The TLC4502 uses a unipolar 5-V supply, has a rail-to-rail output stage, and can be driven down to 0 V at the input. The automatic calibration typically requires 300 ms to activate when the supply voltage is switched on.

Figure 3 shows the block diagram of the TLC4502 compensating circuit. The compensation begins automatically when the supply voltage is switched on. For this purpose, the noninverting input of the op amp is shorted to the inverting input. During this phase, two switches from the normal signal input to the circuit isolate the two inputs. This prevents the common-mode input voltage from influencing the op amp output voltage. The output voltage now corresponds to the op amp input offset voltage (V_{IO}). An internal analog-to-digital converter (ADC) converts the output voltage to digital, and stores the result in a register. The digital data is applied to the integrated digital-to-analog converter (DAC). The DAC output current makes it possible to compensate an input offset voltage of up to 5 mV. During the calibration phase, an RC oscillator provides the necessary clock signal. The oscillator is deactivated as soon as calibration is complete to reduce noise, and to keep down power consumption.

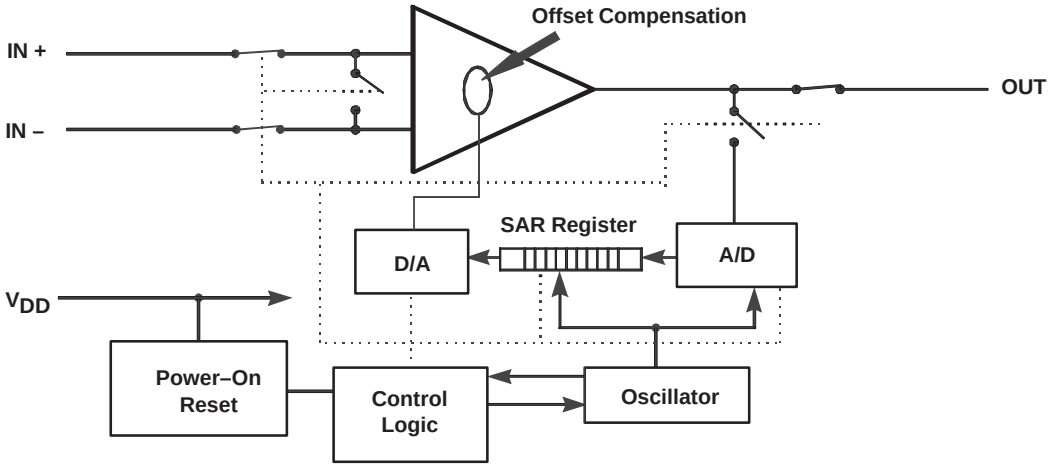

Figure 3. Block Diagram of the TLC4502

Low input offset voltage, reduced temperature drift of the input offset voltage (typically 1 μV/°C), and low input current make the TLC4502 ideal for applications in which small dc voltages must be subjected to high amplification.

Self-Cal is a trademark of Texas Instruments Incorporated.

An Example Unipolar Application

The following application shows the design of a measuring amplifier that uses the TLC4502. This is followed by the solution to the problem of converting the measurement signal from analog into digital in a 10-bit ADC. In this application, a digital signal processor (DSP) controls the ADC.

For amplifying potential differences, such as the diagonal voltage of a Wheatstone bridge, a simple differential amplifier can be used. The differential amplifier is the combination of a noninverting and an inverting amplifier (see Figure 4). Since this circuit has a single supply voltage (5 V), the op amp must have a bias of $V_{CC}/2$ to get the maximum voltage swing at the output. The TLE2425 is ideally suited for this purpose, since it can generate a reference voltage of V_{REF} = 2.5 V from a voltage of 4 V to 40 V. The output voltage of the op amp can then be calculated as follows:

$$V_A = \frac{R_3}{R_1 + R_3} \times \left(1 + \frac{R_4}{R_2}\right) \times V_1 - \frac{R_4}{R_2} \times V_2 + V_{REF}$$

The following expression applies for the calculation of the resistors:

$$\frac{R_4}{R_2} = \frac{R_3}{R_1},$$

so that the following particularly convenient result is obtained:

$$V_A = \frac{R_3}{R_1} \times \left(V_1 - V_2\right) + V_{REF},$$

because with $V_1 = V_2$, the output of the operational amplifier theoretically provides the midpoint voltage V_A = 2.5 V.

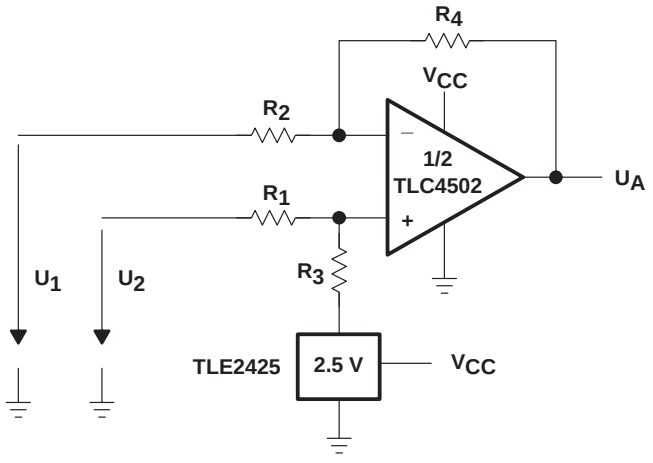

Figure 4. Differential Amplifier

The common-mode rejection of the TLC4502 is typically 100 dB. This means that a common-mode voltage of 1 V has the same effect as a differential voltage of 10 μV between the inputs of the op amp. Changing the ratio of the resistors R4/R2 = R3/R1 has a great influence on the common-mode amplification.

However, the differential amplifier is not suitable for signal sources with high internal resistances. As a result of the finite resistance of the inputs, voltage drops occur in the internal resistance of the source. Very high input resistances can be achieved using two additional op amps. Figure 5 shows this circuit, which is well-known as an instrument amplifier. This circuit uses the previously described differential amplifier, operating with an amplification factor of 1, since all resistors R_3 are the same. Two TLC4502 op amps are connected before the differential amplifier. The signal source (sensor) connected to the instrument amplifier is only loaded with the input resistance of the TLC4502. The typical input resistance of the TLC4502 is $10^{12}\ \Omega$.

Appropriate choice of resistor R_2 adjusts the amplification of the instrument amplifier. The output voltage of the instrument amplifier can be calculated as follows:

$$V_A = (V_2 - V_1) \times \left(1 + \frac{2 \times R_1}{R_2}\right) + V_{REF}.$$

It is important to use high-precision resistors for R_3 to achieve a high common-mode rejection.

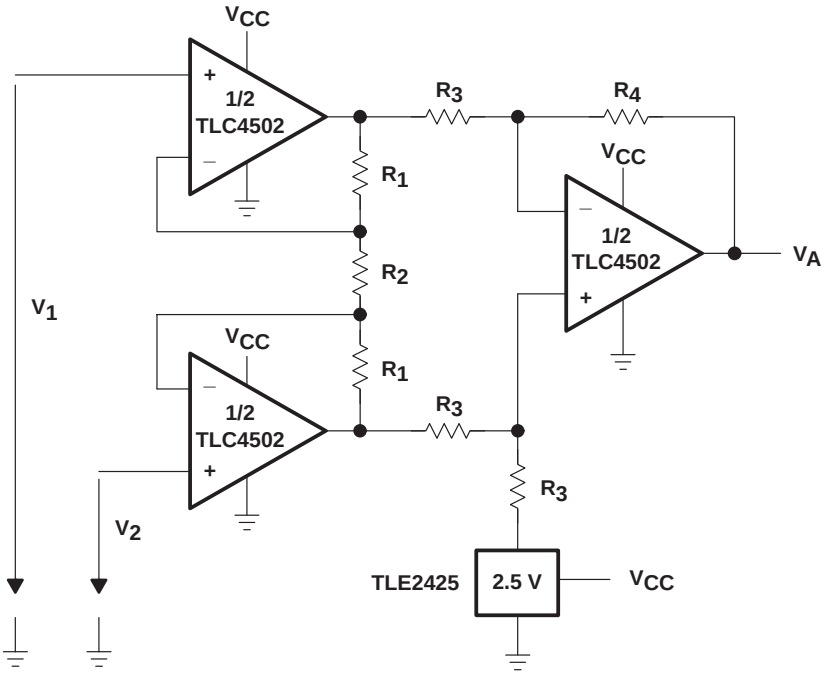

Figure 5. Instrument Amplifier

Analog-to-Digital Conversions

The analog output signal V_A from the differential amplifier or the instrument amplifier must now be converted into a digital signal. To do this, the analog output is connected directly to the analog input of an ADC.

This application uses the TLV1544 (or TLV1548) 10-bit ADC for the conversion. The TLV1544 has four analog inputs; the TLV1548 has eight. Besides the analog input channels, both converters have three self-test channels. The desired channel is activated through the internal multiplexer. These ADCs feature a direct interface to the TMS320 family of DSPs. In addition, they are provided with a direct 3-pole interface to the serial connector of SPI-compatible microprocessors. The TLV1544/8 operates with a supply voltage of from 2.7 V up to 5.5 V, with a low maximum current consumption of only 1 mA. The programmable power-down function reduces the supply current typically to 1 μA. A conversion rate of 85 ksps can be achieved.

In this application the TMS320C542 DSP controls the ADC, and reads out values converted from analog to digital. Figure 6 shows the interface between the ADC and the DSP.

The TMS320C542 serial port (TDM) can be used for control, and for writing in and reading out the conversion values.

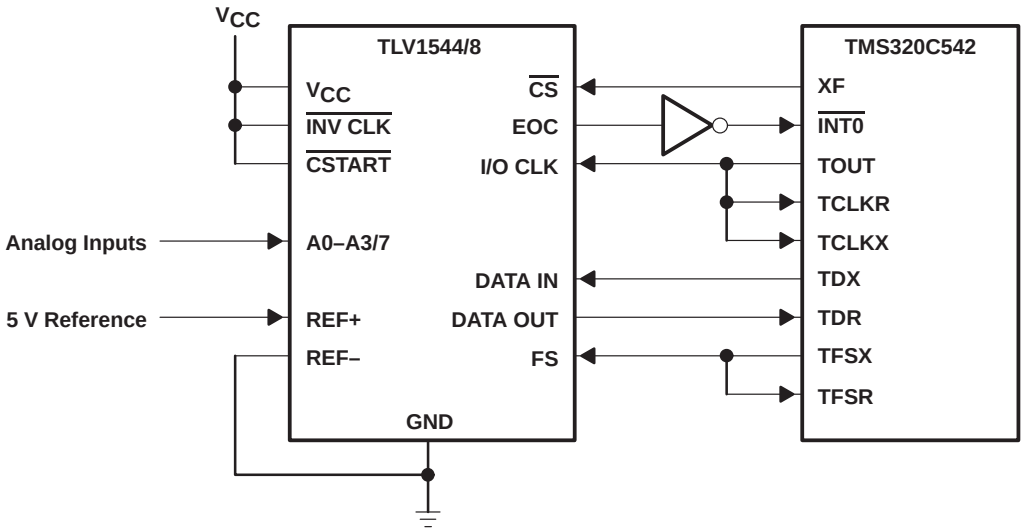

Figure 6. Interface of the TLV1544/8 to the TMS320C542

The DSP XF output signal controls the ADC input chip select ($\overline{CS}$). The DSP TFSX pulse helps initiate the transmission from the DSP. For this to happen, the output must be connected to the TLV1544/8 FS input.

The serial output of the port (TDX) is connected to the data input (DATA IN) of the TLV1544/8. From this output (TDX), the DSP transmits a 4-bit serial data stream to the ADC. These 4 bits contain information for choosing the appropriate analog input, for activating the power-down mode, and for selecting the fast or slow conversion mode.

The serial input of the port (TDR) receives the converted digital values from the data output (DATA OUT). The ADC indicates the end of a conversion cycle with the EOC (end of conversion) output. This signal is inverted and passed to the interrupt input INT0 of the TMS320C542, indicating the end of a conversion cycle. It is now possible to read in the previously converted result, and to continue processing.

The internal timer of the DSP generates the clock signal of the TLV1544/8. For this purpose, the timer output (TOUT) is connected to the clock input (I/O CLK) of the ADC, the maximum clock frequency of which is 8 MHz. The timer output (TOUT) is also connected to the clock inputs of the serial ports (TCLKR and TCLKX).

The inputs REF– and REF+ of the TLV1544/8 determine the upper and lower reference voltages, and thus the maximum input voltage range of the ADC.

Figure 7 shows the timing behaviour at the interface between the ADC and the DSP.

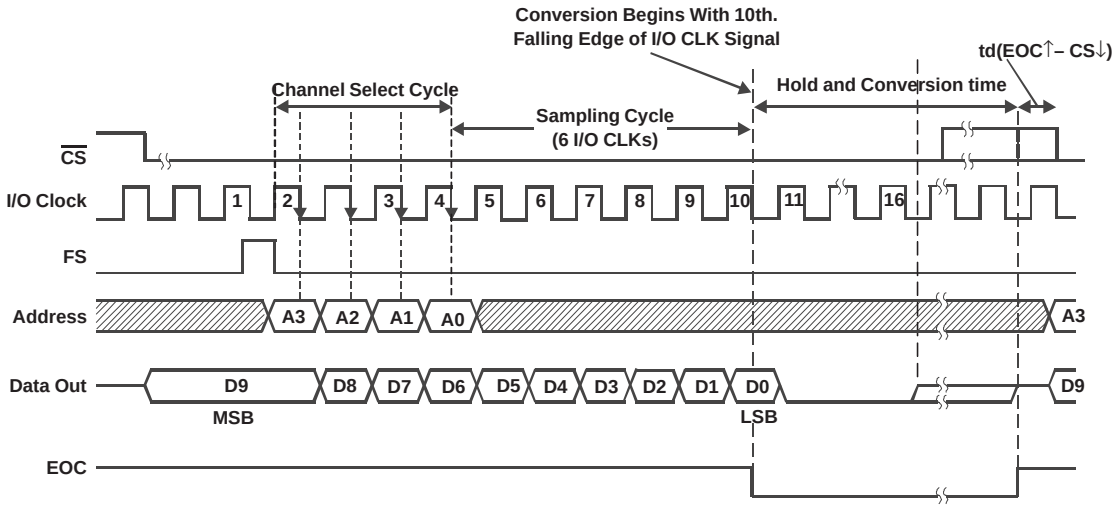

Figure 7. Timing Behavior of the DSP Interface

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